

# **Preliminary Test Plan for Reliability Evaluation of Copper-Based Metallization Systems**

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## **Introduction**

The advantages of using copper for interconnection in microcircuits are mostly due to its lower resistance (bulk resistivity) compared to aluminum metallization. Copper-based metallization has specific resistance of less than  $2\ \mu\Omega\text{-cm}$  compared to more than  $3\ \mu\Omega\text{-cm}$  for aluminum metallization. In combination with a reduced susceptibility to electromigration failures, this low resistivity property enables designing of highly scaled devices with significantly higher performance and reduced RC time delays. These features are mostly beneficial for devices such as high-performance microprocessors and fast static RAMs (FSRAM).

In addition to higher performance, the dual damascene technology incorporating copper interconnect processes, can potentially reduce the manufacturing cost by eliminating some of the labor intensive aluminum etching process steps. This makes copper interconnect technology quite attractive and is listed in the International Technology Roadmap for Semiconductors as the standard interconnect process for most submicron ULSI generation microcircuits and systems-on-chip (SOC) designs in the future.

The reliability evaluation of copper metallization has been mostly focused on electromigration processes in thin copper conductors, due to concerns with reduced size of metallization interconnects in current generation of submicron microcircuits and correspondingly, higher current levels. Several studies performed have shown that copper resistance to electromigration is superior to aluminum.

Major problems with copper metallization are due to its relatively high electrochemical activity (it does not create a passive oxide film as aluminum does), poor adhesion and high rate of diffusion through the silicon and dielectric layers (organic and inorganic). This introduces new failure mechanisms such as poisoning of P-N junctions, charge instability and formation of resistive shorts caused by copper electrochemical migration.

Most studies on copper metallization reliability have been performed using test structures, which focus on a certain mechanism of failure. In real microcircuit applications, different degradation mechanisms may work simultaneously to produce out of specification conditions and failures. Therefore, analysis of actual copper interconnect based parts may provide a better information on their quality and reliability aspects.

The major objective of this evaluation is to gain familiarization with the copper-based design and technology, to develop techniques for deprocessing of the parts, and to obtain preliminary results on the copper interconnect reliability. The amount and extent of actual testing performed will depend on the test equipment available and funding resources.

## Part Description

The part used for this evaluation is copper-based fast SRAM (FSRAM) manufactured by Motorola Corp. The XCM63R836RS3.3 is an 8M-bit synchronous, late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The part is organized as 256K words by 36 bits and is fabricated in Motorola's high performance silicon gate copper CMOS technology (0.15 micron, effective gate length).

The differential clock (CK) inputs control the timing of read/write operations of the RAM. At the rising edge of CK, all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enables the memory to accept write data on the rising edge of CK, a cycle after address and control signals. Read data is also driven on the rising edge of CK. The impedance of the output buffers is programmable, allowing the outputs to match the impedance of the circuit traces, which reduces signal reflections.

The part features low cycle time of 3.3 ns, low power supply voltage of 3.9 V maximum for the core supply voltage and 2.5 V maximum for the output supply voltage. Operating temperature of the part is 0 °C to 70 °C, temperature under bias is -10 °C to 85 °C, and storage temperature is -55 °C to 125 °C.

The part is designed as a Flipped Chip Ceramic Ball Grid Array (CBGA) and Flipped Chip Plastic Ball Grid Array (PBGA). Figure 1 shows external views of the part. The chip is mounted on a ceramic board, using the flip-chip solder bump technology. Bottom side of the board has 119 solder bumps, which are organized in a 17×7 array with a 50 mil (1.27 mm) pitch.

For this evaluation, a total of thirty Motorola FSRAMs (Part No. MCM63R836) were procured, of which twenty are CBGAs and ten are PBGAs. The parts need BGA to PGA translation boards (adapters) for ATE testing and burn-in. Additional fixturing will be required, including burn-in boards.

## **Test Plan FY00**

Due to limited funding, the FY00 test plan includes only destructive part analysis (DPA) of sample Motorola FSRAMs. Copper is much more susceptible to corrosion than aluminum, which requires developing special delayering and cross sectioning techniques. Besides, cross-sectioning of highly scaled devices is always a challenge. Therefore, both, standard cross sectioning techniques and FIB milling techniques, will be developed to analyze quality of copper-based metallization system.

## **Test Plan FY01 (Preliminary)**

### **Electrical testing**

The parts will be subjected to high temperature burn-in testing and measured, using Hewlett-Packard HP82000 automatic tester. For these tests, the parts will have to be mounted (soldered) on to the BGA-to-PGA translation boards (adapters). To perform this testing, software program for HP82000 will have to be developed and burn-in board fixtures will have to be built.

### **Accelerated Aging and Life testing**

The purpose of this testing is to identify problems/weakness of the microcircuits, which are specific to copper metallization. Preliminary analysis shows that copper diffusion and/or migration through defects in the barrier layers might be one of the major failure mechanisms for these devices. Obviously, these failure mechanisms are accelerated by temperature and applied voltage. The most appropriate way to stimulate these mechanisms and to find conditions of their occurrence is to use the step stress profile accelerated testing.

Two groups of devices will be subjected to temperature aging and to burn-in life testing at different temperatures.

#### Temperature Aging Test

The planned test flow for the temperature aging is as follows:

- Initial measurements;
- Aging at 125 °C for 1000 hrs;
- Interim electrical testing;
- Aging at 150 °C for 1000 hrs;
- Interim electrical testing;
- Aging at 175 °C for 1000 hrs;
- Post 1000 hours aging, final electrical testing.

### Burn-in Life Testing

The test flow for the burn-in life testing is as follows:

- Initial measurements;
- BI at 85 °C for 168 hrs;
- Interim electrical testing;
- Aging at 100 °C for 168 hrs;
- Interim electrical testing;
- Aging at 115 °C for 168 hrs;
- Interim electrical testing;
- Aging at 130 °C for 168 hrs;
- Interim electrical testing;
- Aging at 145 °C for 168 hrs;
- Final 1000 hours post-life, electrical testing.

All failed parts will be subjected to failure analysis to ensure that the failures were related to copper metallization.

### **Highly Accelerated Stress Test**

This test will be performed on 10 Motorola FSRAM PBGAs. Figure 2 shows the HAST test flow diagram for the plastic encapsulated modules (PEMS). Figure 3 shows the HAST preconditioning sequence.

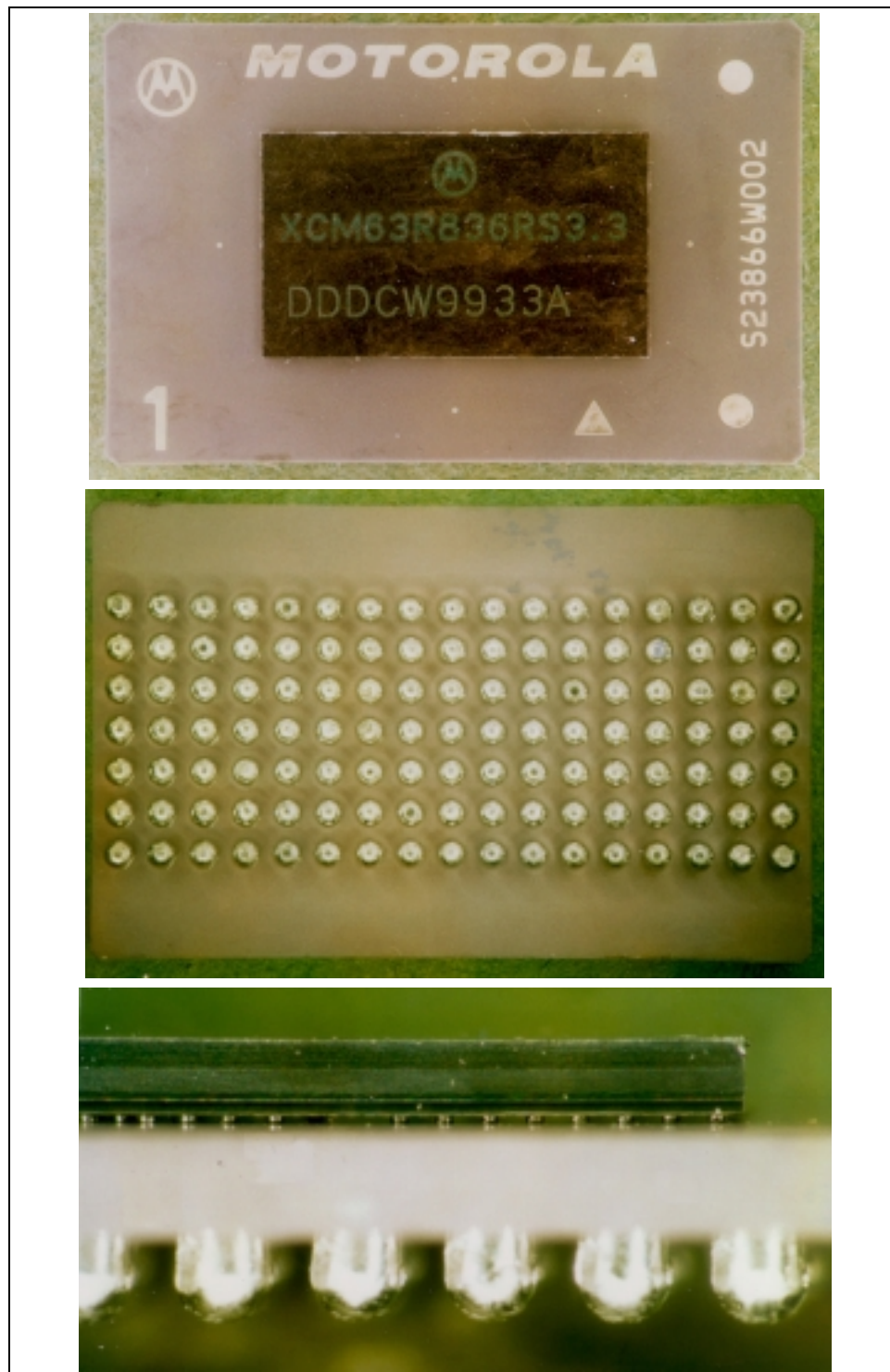


Figure 1. External top, bottom, and side views of the FSRAM.

# HAST TEST FLOW (PEMs)

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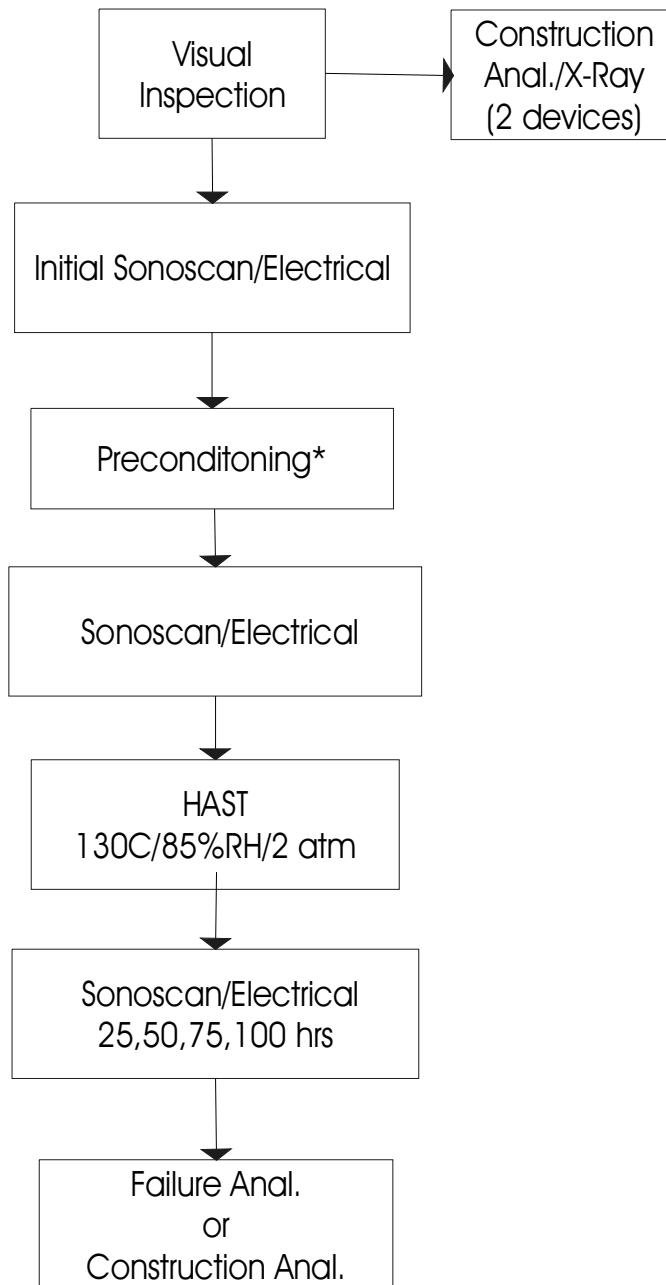


Figure 2 HAST Test Flow (PEMS)

## PRECONDITIONING SEQUENCE

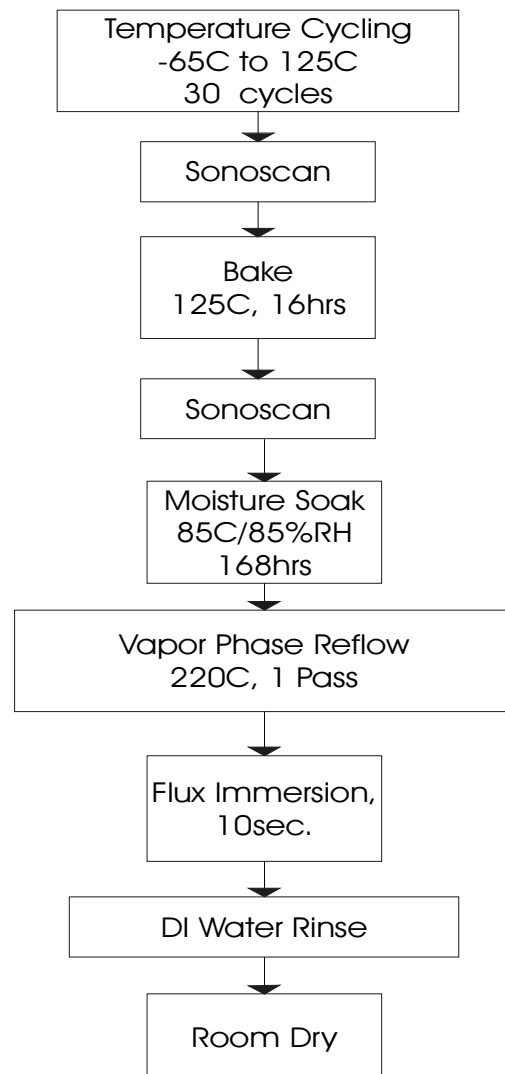


Figure 3 HAST Preconditioning Sequence

Any comments or recommended changes to this test plan should be directed to the points of contacts listed below.

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